REMARKS

Initially, Applicants would like to express appreciation to the Examiner for the detailed Official Action provided, and for the acknowledgment of Applicants' Information Disclosure Statement by return of the Form PTO-1449.

Upon entry of the above amendment, claims 1 and 5 will have been amended. Accordingly claims 1-31 are currently pending. Claims 2-4, 14, 23, 24, and 26 stand withdrawn from consideration by the Examiner as being drawn to a nonelected invention. Applicants respectfully request reconsideration of the outstanding rejection and allowance of claims 1, 5-13, 15-22, 25, and 27-31 in the present application. Such action is respectfully requested and is now believed to be appropriate and proper.

Claims 1, 11-13, 15-22, 29, 30, and 31 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over LI (U.S. 2004/0108581) in view of ISAAK et al. (U.S. 2001/0035572).

Although Applicants do not necessarily agree with the Examiner's rejection of claim 1 on this ground, nevertheless, Applicants have amended independent claim 1 to clearly obviate the above noted ground of rejection in order to expedite prosecution of the present application. In this regard, Applicants note that LI and ISAAK et al. fail to teach or suggest the subject matter claimed in amended claim 1. In particular, claim 1, as amended, sets forth a semiconductor package including, inter alia, a first substrate having a die receiving area, a first adhesive layer, a window opening, and a plurality of conductive traces; a first semiconductor die; a second adhesive layer; "a second substrate having a die receiving area, a plurality of conductive traces and a side with terminals"; a third adhesive layer; "a last semiconductor die, having an electrically active side and an electrically inactive side, the electrically inactive side being mounted to a second side of said third adhesive layer, and the electrically active side being electrically coupled to said conductive traces of said first

or second substrate; a redistribution device that electrically couples the electrically active side of the last semiconductor die to said conductive traces of said first or second substrate"; an encapsulant; and signal transferring interconnections.

This amendment is fully supported by the specification, including the claims and drawings, and no prohibited new matter has been added. In particular, support may be found at least in figure 9 and in the specification in paragraphs [0021] and [0026].

As shown in the embodiment of Figure 9, the semiconductor package of the instant invention includes a first substrate 1 with a die receiving area, a first adhesive layer, a window opening, and a plurality of conductive traces; a first semiconductor chip 3 having the electrically active side mounted to the first substrate 1 through the first adhesive; a second adhesive layer having a first side attached to the electrically inactive side of the first semiconductor chip 3; a second substrate 2 having a die receiving area, a plurality of conductive traces, and a side with terminals; a semiconductor flip-chip 8; a third adhesive layer; and a last semiconductor chip 4 having the electrically inactive side mounted to the second side of the third adhesive layer and the electrically active side electrically coupled to the conductive traces of the first or second substrate directly or through a redistribution device. The semiconductor die 8 is flipped onto the second substrate 2, forming a flip-chip die. The last semiconductor die 4 is attached to the inactive side of the flip-chip die 8.

As recognized by the Examiner in the rejection of dependent claim 5 under 35 U.S.C. § 103(a) over LI in view of ISAAK et al. and further in view of TAO (on page 9 of the Official Action dated May 26, 2010), LI and ISAAK et al. fail to teach or suggest a redistribution device.

Additionally, LI and ISAAK et al. also fail to teach or suggest a redistribution device that couples the electrically active side of a last semiconductor die to conductive traces of said first or second substrate. Accordingly, the LI and ISAAK references fail to teach or suggest a

semiconductor package including, inter alia, "a last semiconductor die, having an electrically active side and an electrically inactive side, the electrically inactive side being mounted to a second side of said third adhesive layer, and the electrically active side being electrically coupled to said conductive traces of said first or second substrate; a redistribution device that electrically couples the electrically active side of the last semiconductor die to said conductive traces of said first or second substrate", as set forth in amended claim 1.

Further, the Examiner has taken the position that the LI publication discloses a second substrate 40 having a die receiving area and a side 56 with terminals; and a last semiconductor die 45 with the electrically active side 48 being electrically coupled to the conductive traces 22a, 22b, 22c of the first or second substrate.

However, Applicants respectfully submit that LI fails to teach or suggest a second substrate having a die receiving area, a plurality of conductive traces, and a side with terminals. The Examiner has read the claimed second substrate on the conductive member 40 of LI. However, LI specifically discloses that the conductive member 40 comprises a "ground plane or an electromagnetic shield" (paragraph [0008]); and that the conductive member 40 comprises "a conductive plate, such as an aluminum plate" (paragraph [0039]. Thus, LI teaches, with particularity, that the conductive member 40 is a solid plate of conductive material, and does not include conductive traces. The Examiner has taken the position that it would have been obvious to substitute conductive traces for the solid conductive plate of LI. However, Applicants respectfully submit that such a substitution would not have been obvious since substituting a conductive trace for the conductive plate in this case is contraindicated. In this regard, the purpose of the conductive member 40 in the LI device is as a grounding or electromagnetic shielding plane. A conductive plate makes a grounding or electromagnetic shielding plane superior to any grounding or electromagnetic shielding that

conductive traces could provide. Accordingly, the purpose of the conductive member 40 of LI of providing a grounding or electromagnetic shielding plane would be better served by a solid plate of conductive material than by a substrate having conductive traces. Therefore, contrary to the Examiner's assertion that the conductive member 40 has conductive traces, it is respectfully submitted that the conductive member 40 of LI is a solid plate of conductive material, and the LI references fails to disclose or teach conductive traces.

Thus, contrary to the Examiner's position, LI does not include a second substrate having a side with terminals and conductive traces. Accordingly, the LI device does not include a semiconductor package including, inter alia, a second substrate having a die receiving area and a plurality of conductive traces and terminal, as set forth in claim 1.

The Examiner has taken the position that it would have been obvious to substitute ISAAK's substrate having a plurality of conductive traces with a side with terminals for LI's substrate.

However, Applicants respectfully submit that LI and ISAAK fail to teach or suggest a second substrate having a die receiving area, a plurality of conductive traces, and a side with terminals. As described in detail above, LI specifically discloses that the conductive member 40 comprises a conductive plate, and not conductive traces. Accordingly, the conductive member 40 of LI is a solid plate of conductive material, and the conductive member 40 does not include conductive traces. Moreover, the purpose of the conductive member 40 in the LI device is as a grounding or electromagnetic shielding plane. Such a purpose would not be served by a substrate having conductive traces, as in the ISAAK device. Therefore, contrary to the Examiner's assertion that it would have been obvious to substitute ISAAK's substrate having a plurality of conductive traces with a side with terminals for LI's substrate, it is respectfully submitted that it would not have been obvious to make such a substitution. In fact, the LI and ISAAK references teach away from such a

substitution since providing the LI conductive member 40 with conductive traces is contraindicated, as described above.

Accordingly, in view of all of the above, LI fails to teach or suggest the semiconductor package as claimed, and ISAAK et al. fails to cure the deficiencies of the LI device. Thus, even assuming, arguendo, that the teachings of LI and ISAAK et al. have been properly combined, Applicant's claimed semiconductor package would not have resulted from the combined teachings thereof.

Further, there is nothing in the cited prior art that would lead one of ordinary skill in the art to make the modification suggested by the Examiner in the rejection of claim 1 under 35 U.S.C. § 103(a) over LI in view of ISAAK et al. Thus, the only reason to combine the teachings of LI and ISAAK et al. results from a review of Applicants' disclosure and the application of impermissible hindsight. Accordingly, the rejection of claim 1 under 35 U.S.C. § 103(a) over LI in view of ISAAK et al. is improper for all the above reasons and withdrawal thereof is respectfully requested.

Additionally, in the rejection of claim 5 under 35 U.S.C. § 103(a) over LI in view of ISAAK et al. and further in view of TAO, the Examiner has taken the position that the TAO et al. patent discloses bond pads 407 not positioned near the periphery of a last semiconductor die 401 and that the bond pads 407 are relocated to the periphery by a redistribution device 406; and that it would have been obvious to include redistribution devices as taught by TAO et al. in the LI device with predictable results.

However, Applicants respectfully submit that the elements in combination do not merely perform the function that each element performs separately. In this regard, the Examiner has taken the position that providing the LI device with a redistribution device would have produced predictable results. However, the combination as proposed by the Examiner would still not provide

the apparatus as claimed. In particular, claim 1, as amended, sets forth that the redistribution device electrically couples the electrically active side of the last semiconductor die to the conductive traces of the first or second substrate. However, merely adding a redistribution device, as suggested by the Examiner, would not add a redistribution device with the particular claimed configuration, connections, and electrical coupling. Moreover, the redistribution device, the electrically active side of the last semiconductor, and the conductive traces of the first and second substrate all cooperate together with particularity in the instant invention to perform the function that is particular to the instant invention. That is, the electric coupling of the electrically active side of the last semiconductor die to conductive traces of a first or second substrate. Accordingly, the elements in combination do not merely perform the function that each element performs separately.

Therefore, a rejection of claim 1 under 35 U.S.C. § 103(a) over LI in view of ISAAK et al. and further in view of TAO et al. would be improper.

Applicants submit that dependent claims 5-13, 15-22, 25, and 27-31, which are at least patentable due to their dependency from claim 1 for the reasons noted above, recite additional features of the invention and are also separately patentable over the prior art of record based on the additionally recited features.

In particular, Applicants submit that none of the cited prior art teaches or suggests a semiconductor package including "where said last semiconductor die has a plurality of bond pads, whereby said bond pads are not positioned near the periphery of said last semiconductor die, said bond pads being electrically relocated to the periphery of said last semiconductor die by said redistribution device", as set forth in claim 5. None of the cited prior art teaches or suggests a semiconductor package including "wherein said redistribution device includes a wafer redistribution layer", as set forth in claim 6. None of the cited prior art teaches or suggests a semiconductor

package including "wherein said redistribution device includes a metallic interposer with a plurality of conductive traces, attached to the active surface of the last semiconductor die with an adhesive, with a plurality of electrical couplings from the bond pads to the metallic interposer", as set forth in claim 7. In this regard, it is noted that the TAO device fails to teach or suggest the particulars of the redistribution device including the bond pads being electrically relocated by the redistribution device; a wafer redistribution layer; and a metallic interposer with a plurality of conductive traces, attached to the die with an adhesive and electrical couplings from bond pads to the metallic interposer, as set forth in the dependent claims. Accordingly, claims 5-13, 15-22, 25, and 27-31 are each separately patentable for these additional reasons.

Accordingly, Applicants respectfully request reconsideration and withdrawal of the rejections, and an early indication of the allowance of claims 1, 5-13, 15-22, 25, and 27-31.

SUMMARY AND CONCLUSION

In view of the foregoing, it is submitted that the present response is proper for entry since it merely clarifies the language describing the electrical coupling of the last semiconductor die to conductive traces of the first or second substrate by the redistribution device, which is an issue about which Applicants have already presented arguments, and it is also submitted that none of the references of record, considered alone or in any proper combination thereof, anticipate or render obvious Applicants' invention as recited in claims 1, 5-13, 15-22, 25, and 27-31.

Accordingly, consideration of the present response, reconsideration of the outstanding Official Action, and allowance of all of the claims in the present application are respectfully requested and now believed to be appropriate.

Applicants have made a sincere effort to place the present application in condition for allowance and believe that they have now done so.

Should the Examiner have any questions, the Examiner is invited to contact the undersigned at the below-listed telephone number.

Respectfully submitted,
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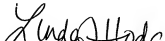

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